Unique Paper Code   : 32341102-OC

Name of the Paper   : Computer System Architecture

Name of Course   : B.Sc. Hons. Computer Science

Semester   : I

Duration of Examination   : Three Hours

Maximum Marks   : 75 Marks

(For students admitted in 2015, 2016, 2017 & 2018)

Instructions for Candidates:

1. Answer any **FOUR** questions out of **SIX**.
2. All questions carry equal marks.

1. Design a combinational circuit with three binary inputs a, b & c and three binary outputs x, y & z. When the binary input has even number of 1's, then the output is one more than the input. When the binary input has odd number of 1's, then the output is one less than the input. The output remains the same if the input is zero.
   Redraw the above designed circuit using NAND gates only.
   Explain the functionality and disadvantage of SR flip-flop.

2. A two-word instruction at address 300 and 301 is a "load to AC" instruction with an address field equal to 400. The first word of the instruction specifies the operation code and mode, and the second word specifies the address part. PC has the value 300 for fetching the instruction. The content of processor register R1 is 500, and the content of index register XR is 200. Consider the following memory state:

Address	Memory	
300	Load to AC	Mode
301	400	
400	425	
425	450	
499	525	
500	550	
501	575	
600	650	
700	725	
701	726	
702	750	
900	925	
925	950	

The content of R1 is incremented and decremented prior to the execution of the instruction in case of autoincrement and autodecrement respectively. Show the content of AC in case of following addressing mode:

- Indirect
- Relative
- Indexed
- Register
- Autodecrement

What would be the content of R1 after the execution of instruction Autoincrement?

3. The content of AC in hexadecimal is BF43 and the initial value of E is 1. The initial value of PC in hexadecimal is 08F. The three instructions (CIR, SNA & CMA) will execute in the following sequence:

<div align="center">

CIR
SNA
CMA

</div>

Determine the contents of AC, E, PC, AR and IR in hexadecimal after the execution of every instruction. [Hint: The operation code for CIR is 7080, SNA is 7008 & CMA is 7200.]

4. Perform the arithmetic operation (-54) - (-35) in binary using signed 2's complement representation for the negative numbers.
Perform the following conversions to the indicated bases:
   - $(973456)_{10}$ $= (?)_6$
   - $(FE123)_{16}$ $= (?)_8$
   - $(101110.101)_2$ $= (?)_{10}$

Give the logic diagram and truth table of a 3-to-8-line decoder using NAND gates only. Include an active low enable input.

5. In a certain scientific computation, it is necessary to perform the arithmetic operation $(A_i * B_i) + (C_i * D_i)$ with a stream of numbers. Using a diagram of combinational circuit, specify a pipeline configuration to carry out this task. Assuming that there are 6 tasks for the given computation, list the contents of all registers in the pipeline for $i = 1$ through 6 with the help of a table. Draw a space time diagram for this pipeline.

6. Assuming 5-bit registers that hold signed numbers, show the step-by-step multiplication process using Booth algorithm when numbers (-8) & (-12) are multiplied in binary.
Also perform the division of 0101010 by 111. (Both the dividend and divisor are fixed-point binary number in signed magnitude representation)